Agile for EMBEDDED SYSTEMS

- □ 1st-generation systems used hardwired logic
- □ 2nd-generation systems used PROMS & FPGAs
- ¬ ard-generation systems use APP. SW & COTS HW

Iterations, Integrations, & Validations

AGILE "Software Model" - MOST FLEXIBLE -



- Least Cost
- Lowest Risk
- → 90% Software
 - COTS Hardware
 - Early, Iterative Dev.
- Continuous V&V

NEO-TRADITIONAL "FPGA Model" - MALLEABLE -

- Moderate Lead
- Moderate Cost
- Moderate Risk
- 50% Hardware
- COTS Components
- Midpoint Testing
- "Some" Early V&V

TRADITIONAL "Hardwired Model" - Least Flexible -

- Long Lead
- Highest Cost
- Highest Risk
- 90% Hardware
- Custom Hardware
- Linear, Staged Dev.
- Late Big-Bang I&T

RISK Embedded Systems More HW Than SW











GOAL — SHIFT FROM LATE HARDWARE TO EARLIER SOFTWARE SOLUTION

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